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09/914,118	08/23/2001	Gene Karl Sendelweck	RCA 89226	9587

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EXAMINER	
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ART UNIT	PAPER NUMBER
2614	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/914,118	Applicant(s) SENDELWECK, GENE KARL	
	Examiner Trang U. Tran	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 29, 2004 have been fully considered but they are not persuasive.

In re pages 6-7, applicant argues that, with respect to claim 1, that Anderson uses four transistors each having only a single input which is responsive to a signal while the claim 1 recites a generator of a scanning velocity modulation deflection signal comprising a variable conduction device that itself comprises a single transistor (Q1) having a first input (Q1e) responsive to a negative feedback signal CS1 representative of scanning velocity modulation deflection poser and a second input (Q1b) responsive to a control signal CS2.

In response, the examiner respectfully disagrees. First at all, claim 1 recites a generator of a scanning velocity modulation deflection signal, **comprising**: a variable conduction device **comprising** a transistor ... Because the transitional phrase "**comprising**", claim 1 does not limit to **only** one transistor. Transistor 51 of Anderson has a first input (emitter) responsive to a negative feedback signal and a second input (base) responsive to a control signal and operates in two conditions, in a first condition the transistor providing a path for said negative feedback signal for controlling said scanning velocity modulation deflection signal in magnitude and, in a second condition the transistor interrupting said path and substantially inhibiting generation of said scanning velocity modulation deflection signal.

In re page 7, applicant states that claims 2-6 depend from claim 1 and are, for the same reasons not anticipated by Anderson.

In response, as discussed above with respect to claim 1, Anderson discloses all the claimed limitations of claim 1.

In re pages 7-8, applicant argues that although the use of variable conduction states is known, applicant's inventive arrangement substantially inhibits generation of the scanning velocity modulation deflection signal in a manner (by saturated conduction of transistor Q1) which is completely contrary to the action of Anderson where transistor 65 is turned off to inhibit signal generation, furthermore, when transistor 65 of Anderson is fully conductive the SVM deflection signal is maximized not inhibited, Anderson offers no motivation to one of ordinary skill to modify the circuitry to provide applicant's recited signal inhibition by use of a fully conductive device, and Anderson offers no teaching nor motivation to enable one of ordinary skill to modify Anderson's arrangement to provide the recited features of applicant's claims 4 and 5.

In response, the examiner respectfully disagrees. First at all, claims 4-5 have been amended to "wherein during said second condition said transistor is fully conductive .....substantially inhibiting said scanning velocity modulation deflection signal". Because of the amendments, the rejection of claims 4-5 under 35 U.S.C. § 103(a) is herein withdrawn and the new ground of rejection of claims 4-5 under 35 U.S.C. § 102(b) is applied. Finally, during the second condition, the scanning velocity modulation deflection signal of Anderson **would inhibited when the transistor 51 is fully conductive and transistor 65 is disabled**.

Thus, Anderson does indeed disclose the claimed limitations of the amended claims 4-5.

In re page 8, applicant argues that claim 8 is allowable for the same reasons as discussed in claim 1 above.

In response, as discussed above, Anderson discloses all the claimed limitations of claim 1.

In re page 8, applicant argues that Anderson does not teach or suggest the use of a transistor configured as applicant's claim 9 for selectable operation as either a common emitter or common base amplifier but, indeed, each of Anderson's transistors 65, 118, 133, and 136 only operate in a common emitter configuration.

In response, the examiner respectfully disagrees. As discussed above with respect to claim 1, Anderson's transistor 51 anticipates the claimed transistor because transistor 51 has two inputs (emitter and base) and operates in two conditions.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 and 8-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (US Patent No. 5,072,300).

In considering claim 1, Anderson discloses all the claimed subject matter, note 1) the claimed a variable conduction device comprising a transistor coupled to said generator and having a first input responsive to a negative feedback signal and a second input responsive to a control signal is met by the differential limiting amplifier 32 which includes the current source transistor 65 (Figs. 1 and 3, col. 4, lines 19-68 and col. 5, line 48 to col. 7, line 39), 2) the claimed in a first condition said transistor providing a path for said negative feedback signal for controlling said scanning velocity modulation deflection signal in magnitude is met by the base electrode of current source transistor 65 is coupled to the collector electrode of a control transistor 118, for controlling the current through limiting amplifier 32 (Figs. 1 and 3, col. 4, lines 19-68 and col. 5, line 48 to col. 6, line 4), and 3) the claimed in a second condition said transistor interrupting said path and substantially inhibiting generation of said scanning velocity modulation deflection signal is met by the base electrode of current source transistor 65 is coupled to the collector electrode of transistor 136 via resistor 135 and any given one of blanking pulses 40a will switch on transistor 136 for the duration of that pulse, rapidly discharging capacitor 137, diverting base current from transistor 65 which made the current source for differential amplifier 32 is turned off or substantially reduced in magnitude (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

In considering claim 2, the claimed wherein during said first condition said transistor varies conduction in accordance with a magnitude of said negative feedback signal is met by the base electrode of current source transistor 65 is coupled to the collector electrode of a control transistor 118, for controlling the

current through limiting amplifier 32 and this control varies the peak-to-peak output signal of the limiter (Figs. 1 and 3, col. 4, lines 19-68 and col. 5, line 48 to col. 6, line 4).

In considering claim 3, the claimed wherein said transistor varies conduction to variably attenuate a scanning velocity modulating signal in accordance with said negative feedback signal magnitude is met by the base electrode of current source transistor 65 is coupled to the collector electrode of a control transistor 118, for controlling the current through limiting amplifier 32 and this control varies the peak-to-peak output signal of the limiter (Figs. 1 and 3, col. 4, lines 19-68 and col. 5, line 48 to col. 6, line 4).

In considering claim 4, the claimed wherein during said second condition said transistor is fully conductive responsive to said control signal for substantially inhibiting said scanning velocity modulation deflection signal is met by the base electrode of current source transistor 65 is coupled to the collector electrode of transistor 136 via resistor 135 and any given one of blanking pulses 40a will switch on transistor 136 for the duration of that pulse, rapidly discharging capacitor 137, diverting base current from transistor 65 which made the current source for differential amplifier 32 is turned off or substantially reduced in magnitude (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

In considering claim 5, the claimed wherein during said second condition said transistor is fully conductive, attenuating said negative feedback signal and substantially inhibiting generation of said scanning velocity modulation deflection signal is met by the base electrode of current source transistor 65 is coupled to

the collector electrode of transistor 136 via resistor 135 and any given one of blanking pulses 40a will switch on transistor 136 for the duration of that pulse, rapidly discharging capacitor 137, diverting base current from transistor 65 which made the current source for differential amplifier 32 is turned off or substantially reduced in magnitude (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

In considering claim 6, the claimed wherein said second condition conduction in said transitor is unresponsive to said negative feedback signal is met by the base electrode of current source transistor 65 is coupled to the collector electrode of transistor 136 via resistor 135 and any given one of blanking pulses 40a will switch on transistor 136 for the duration of that pulse, rapidly discharging capacitor 137, diverting base current from transistor 65 which made the current source for differential amplifier 32 is turned off or substantially reduced in magnitude (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

Claim 8 is rejected for the same reason as discussed in claim 1.

Claim 9 is rejected for the same reason as discussed in claim 1.

In considering claim 10, the claimed wherein said negative feedback signal is representative of power dissipation in a scanning velocity modulation drive amplifier responsive to said scanning velocity modulation deflection signal is met by the base electrode of current source transistor 65 is coupled to the collector electrode of transistor 136 via resistor 135 and any given one of blanking pulses 40a will switch on transistor 136 for the duration of that pulse, rapidly discharging capacitor 137, diverting base current from transistor 65 which

made the current source for differential amplifier 32 is turned off or substantially reduced in magnitude (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

Claim 11 is rejected for the same reason as discussed in claim 5.

Claim 12 is rejected for the same reason as discussed in claim 10.

In considering claim 13, the claimed wherein said common emitter amplifier substantially inhibits generation of said scanning velocity modulation deflection signal by attenuating a signal input to said generator is met by the common emitter of the transistor amplifier 32 (Figs. 1 and 3, col. 6, line 5 to col. 7, line 39).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (703) 305-0090. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT TT
July 10, 2004

MICHAEL H. LEE
PRIMARY EXAMINER